AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-2. (cancelled).

3. (original): A display control circuit for inputting input video data that is composed of parallel data to transfer video data obtained by serializing each piece of the input video data in a two-bit unit of a first bit and a second bit as output video data to a signal-line driving circuit, said display control circuit characterized in having:

first comparison determination means for comparing a noninversion bit of the second bit of previous data with a noninversion bit of the first bit of subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

second comparison determination means for comparing an inversion bit of the second bit of the previous data with the noninversion bit of the first bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

fourth comparison determination means for comparing the inversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

selection means that is composed of first selection means and second selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, and the output of either of the determination results of said third comparison determination means and said fourth comparison determination means respectively, said first selection means being controlled by the output of the second selection means based on of the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means;

output means for, based on the output of said first selection means and the output of said second selection means of said selection means, making an inversion or a noninversion of the first bit of the subsequent data and the second bit of the subsequent data respectively to output them, and for outputting an inversion signal indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit for serializing the output of said output means in a two-bit unit to output it as the output video data and an output inversion signal.

4. (previously presented): A display control circuit comprising:

a first comparator which is configured to compare a noninversion bit of the 2^m-th bit of previous data having a 2^m-bit unit with the noninversion bit of the first bit of subsequent data having a 2^m-bit unit to determine whether the bit inversion number is more than half,

a second comparator which is configured to compare an inversion bit of the 2^m-th bit of the previous data having a 2^m-bit unit with the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit to determine whether the bit inversion number is more than half,

a third comparator which is configured to compare the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the second bit of the subsequent data having a 2^m-bit unit to determine whether the bit inversion number is more than half;

a fourth comparator which is configured to compare the inversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the second bit of the subsequent data having a 2^m-bit unit to determine whether the bit inversion number is more than half;

$2 \times 2^{m-1}$-th comparators which are configured to compare the noninversion bit of the 2^{m-1}-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether the bit inversion number is more than half,

2×2^m-th determining units which are configured to compare the inversion bit of the 2^{m-1}-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether the bit inversion number is more than half;

a selector comprising a first selector, a second selector, ..., and a 2^m-th selector, which are configured to select and output the output of either of the determination results of said first and second determining units, the output of either of the determination results of said third and fourth determining units, ..., and the output of either of the determination results of said $2 \times 2^{m-1}$-th and said 2×2^m-th comparators, respectively, said first selector being controlled by the output of the 2^m-th selector based on the input video data that is one piece of the data ahead, said second

selector being controlled by the output of the first selector, ..., said 2^m-th selector being controlled by the output of the 2^{m-1}-th selector;

an output circuit, which is configured to, based on the outputs of said first selector, said second selector, ..., and said 2^m-th selector of said selectors, make an inversion or a noninversion of the first bit, the second bit, ..., and the 2^m-th bit of said subsequent data, respectively, and to output them along with an inversion signal indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit which is configured to serialize the output of said output means in a 2^m-bit unit and to output the serialized data as the output video data and an output inversion signal.

5. (original): A liquid crystal display device comprising: a display control circuit for inputting input video data that is composed of parallel data to transfer video data obtained by serializing each piece of the input video data in a two-bit unit of a first bit and a second bit as output video data; and a signal-line driving circuit for inputting said output video data, said liquid crystal display device characterized in that said display control circuit comprises:

first comparison determination means for comparing a noninversion bit of the second bit of previous data with the noninversion bit of the first bit of subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

second comparison determination means for comparing an inversion bit of the second bit of the previous data with the noninversion bit of the first bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

fourth comparison determination means for comparing the inversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

selection means that is composed of first selection means and second selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, and the output of either of the determination results of said third comparison determination means and said fourth comparison determination means respectively, said first selection means being controlled by the output of the second selection means based on the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means;

output means for, based on the output of said first selection means and the output of said second selection means of said selection means, making an inversion or a noninversion of the first bit of the subsequent data and the second bit of the subsequent data respectively to output them, and for outputting an inversion signal indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit for serializing the output of said output means in a two-bit unit to output it as the output video data and an output inversion signal.

6. (original): A liquid crystal display device comprising a display control circuit as claimed in claim 4.

Claim 7. (cancelled).

8. (previously presented): A display control circuit comprising:

a first comparator which is configured to compare a noninversion bit of second bits of a first data with a noninversion bit of first bits of a second data following said first data to output a first determination result as to whether the bit inversion number is more than half;

a second comparator which is configured to compare an inversion bit of said second bits of said first data with the noninversion bit of said first bits of said second data to output a second determination result as to whether the bit inversion number is more than half;

a third comparator which is configured to compare the inversion bit of first bits of said second data with the noninversion bit of the second bits of said second data to output a third determination result as to whether the bit inversion number is more than half;

a fourth comparator which is configured to compare the inversion bit of said first bits of said second data with the noninversion bit of the second bits of said second data to output a fifth determination result as to whether the bit inversion number is more than half;

a first selector which is configured to selectively output one of said first and second determination results, said first selector being controlled by the output of a second selector;

a second selector which is configured to selectively output one of said third and fourth determination results, said second selector being controlled by the output of the first selector;

an output circuit which is configured to output an inversed signal or a non-inverted signal of the first bits of the second data based on the output of said first selector and an inversed signal

or a non-inverted signal of the second bits of the second data based on the output of said second selector, and to output an inversion signal indicating the inversion or non-inversion; and

a parallel-to-serial conversion circuit which is configured to serialize the output of said output circuit in a two-bit unit to output it as the output video data and an output inversion signal.

9. (previously presented): A liquid crystal display device comprising the display control circuit as claimed in claim 8.

Claims 10-17 (cancelled).